IN THE CLAIMS:

Please amend the claims as follows:

1. (Previously amended) A DMA controller capable of generating ring buffer addresses, comprising:

a first register, which, in a first mode of operation, sets the start address of a ring buffer,

a second register, which, in said first mode of operation, sets the number of DMA transfers from the start address to the end address of the ring buffer, and

a third register, which, in said first mode of operation, contains a value corresponding to the difference between the end address and the start address of the ring buffer.

2. (Previously amended) The DMA controller according to claim 1, wherein, in a second mode of operation, the second register is used as a register for setting the number of DMA transfers in a contiguous area including rectangular areas in the DMA transfer of a rectangular area included in an area.

3. (Previously amended) The DMA controller according to claim 1 or 2, wherein, in said second mode of operation, the third register is used as a register for setting the address increment of a non-contiguous area in the DMA transfer of a rectangular area included in an area.

4. (Previously amended) The DMA controller according to any of claims 1 through 2, further comprising:

a fourth register, which retains a current transfer address,

a counter, which counts the number of DMA transfers set to the second register, and

an adder, which sums the value of the third register and the value of the fourth register when the counter has completed counting the number of DMA transfers set to the second register.

5. (Currently amended) A computer readable medium encoded with a computer program for executing DMA transfer to a ring buffer, wherein, in the case of ring buffer transfer, the program causes a computer to work as means for setting the start address of a ring buffer to a first register, means for setting the number of DMS transfers from the start address to the end address of the ring buffer to a second register, and means for setting the difference between the end address and the start address of the ring buffer to a third register,

and in the case of rectangular block transfer, said program causes the computer to work as the means for setting the start address at the start of the transfer to said first register, means for setting the number of DMA transfers in a contiguous area including rectangular areas to [[a]] the second register, and means for setting the address increment of a non-contiguous area to the third register.

6. (Previously presented) The DMA controller according to claim 3, wherein said first mode of operation corresponds to a ring buffer transfer, and said second mode of operation corresponds to a rectangular block transfer.